REMARKS

Claims 1-22 are pending in this application. Claims 1, 12 and 18 have been amended. New claims 21 and 22 have been added. A Request for Continued Examination is submitted herewith. Reexamination and reconsideration of the amended application respectfully is requested.

Claim 18 has been amended by canceling the duplicated term "signal" at the end of the claim as suggest by Examiner. The objection to this claim accordingly should be withdrawn

Rejections under 35 U.S.C. 103(a)

Claims 1-7 and 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (*AAPA*). Claim 1 and 12 have been amended and the rejection is inapplicable to the amended claims 1 and 12 and depending claims 2-7 and 13-16, respectively.

Claims 1 and 12 have been amended to clarify that the step of "transforming the voltage level of the optimization verification signal to a second voltage level" is performed "*according to the bus connection signal.*" This amendment is supported in the original application.

Thus, as described at page 8, lines 13-16 of the specification, a signal with a logic level "1" is input to the input terminal 42A of the OR logic gate 42 in the signal level detection circuit 21, so that the terminal Q of the flip-flop 40 *outputs a signal LDTSTOP_STATUS* (optimization verification signal) with logic level "1" (first voltage level). As described at page 8, lines 27-29 and page 9, lines 1-2 of the specification, when the signal LDTSTOP# is asserted to a low voltage level (bus connection signal), the logic level of the signal LDTSTOP_STATUS (optimization verification signal) output from the terminal Q of the flip-flop 40 is cleared to "0" (transforming the voltage level of the optimization verification signal to a second voltage level). Applicants believe that

the above clearly fully supports the limitation of "transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal."

Claims 1 and 12 have been amended also to clarify that the "reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal" is performed "*with the logic level transformed to the second voltage level.*" Applicants believe that the limitation of "reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic level transformed to the second voltage level" is supported in the specification. Thus, the specification at page 9, lines 6-7 describes that the CPU determines whether the voltage level of the signal LDTSTOP_STATUS (optimization verification signal) is "0" (second voltage level). Moreover, the specification at page 9, lines 9-10 describes that the LDT bus connected between CPU and the Northbridge is reconnected when the voltage level of the signal LDTSTOP_STATUS (optimization verification signal) is "0" (second voltage level).

Claim 1, as amended, recites a method for verifying optimization of a processor link for a system that has a Northbridge, a bus coupled between a CPU and the Northbridge, and a Southbridge. The claimed method includes the steps of setting an initial bus width and an initial bus frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency; generating a read request to read the Southbridge; outputting a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receives the read request, initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level; outputting a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal; and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic

level transformed to the second voltage level, wherein the bus operates thereafter at another bus operating bus width and another bus operating frequency.

Claim 12, as amended, also recites a method for verifying optimization of a processor link for a system having a Northbridge, a bus coupled between the CPU and the Northbridge, and a Southbridge. The method of claim 12 includes the steps of setting an initial bus width, an initial bus frequency, a bus operating bus width and a bus operating frequency of the bus coupled between the CPU and the Northbridge, wherein the bus operates at the initial bus width and the initial bus frequency; setting an optimized bus operating bus width and an optimized bus operating frequency of the bus; generating a read request to read the Southbridge; outputting a bus disconnection signal by the Southbridge to disconnect the CPU and the Northbridge when the Southbridge receiving the read request, initializing a timer for calculating an elapsed time value and outputting an optimization verification signal with a first voltage level; outputting a bus connection signal by the Southbridge when the elapsed time value reaches a predetermined value; transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal; and reconnection of the CPU and the Northbridge by the bus according to the optimization verification signal with the logic level transformed to the second voltage level, wherein the bus operates thereafter at the optimized bus operating bus width and the optimized bus operating frequency.

Applicants respectfully disagree with the Examiner's position that all of the claimed method steps are disclosed by or obvious from *AAPA*. Clearly, *AAPA* does not teach or suggest output of ***both*** a bus disconnection signal by the Southbridge and an optimization verification signal with a first voltage level. *AAPA* discloses only output of a bus disconnection signal (LDTSTOP# with low voltage level), with no additional optimization verification signal generated. For this reason alone, the Applicants believe that claims 1 and 12 are allowable over *AAPA*, so that the rejection of claims 1 and 12 should be withdrawn.

In addition, *AAPA* does not teach or suggest ***transforming the voltage level of the optimization verification signal to a second voltage level according to the bus connection signal.*** *AAPA* discloses only generation of a bus connection signal (LDTSTOP# with high voltage level) by transformation the voltage level of the *bus disconnection signal*, **not** transformation of the voltage level of the ***optimization verification signal.***

Note that the bus disconnection signal (LDTSTOP# with low voltage level) or bus connection signal (LDTSTOP# with high voltage level) and the optimization verification signal are different signals, such that no optimization verification signal is disclosed in *AAPA*, which thereby neither teaches nor suggests transformation of the voltage level of the optimization verification signal to a second voltage level ***according to the bus connection signal.*** For this reason also, the Applicants believe that claims 1 and 12 are allowable over *AAPA*, so that the rejection of Claims 1 and 12 should be withdrawn.

Claims 8-11 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (*AAPA*) in view of *Habid et al.* (US 6903583). The rejection respectfully is traversed.

Claim 8, depending on claim 1, recites the optimization verification signal is output by a signal level detection circuit. Claim 17, depending on claim 12, recites the optimization verification signal is output by a signal level detection circuit.

Upon a careful reading the cited reference it will be noted that according to the teachings of *Habid et al.,* the power supply shutdown control prevents the power supply from being turned back on before the output voltages have reached a sufficiently low voltage level (see abstract of *Habid et al.*). However, the problem faced in *AAPA* is to detect completion of the asserted and de-asserted signal LDTSTOP# sequences (see page 4, lines 12-13 of the specification), **not** to monitor and turn on power immediately after the power is turned off to provide a good protection for a system.

Thus, the problems solved by *AAPA* and *Habid et al.* are different. **Clearly then motivation to combine *AAPA* and *Habid et al.* does not exist.** It would appear to the Applicants that the Examiner has combined these two references based only on his having first read the Applicants' disclosure, and that the conclusion of obviousness therefore is based upon "impermissible hindsight."

For this reason alone, claims 8 and 17 are patentable over the cited art. Moreover claims 8 and 17 depend from claims 1 and 12, and *Habid et al.* fail to disclose the features of claim 1 missing from *AAPA*. Therefore, for these reasons the claims are deemed to be clearly patentable and the rejection accordingly should be withdrawn. Further, insofar as claims 9-11 depend on claim 8 and claims 19 and 20 depend from claim 17, these claims also are allowable.

Still further, it is noted that claim 11, depending from claims 1 and 8, recites a signal level detection circuit coupled to the input terminals of the CPU or the Northbridge, and that claim 20, depending from claims 17 and 12, recites a signal level detection circuit coupled to the input terminals of the CPU or the Northbridge. Neither *AAPA* nor *Habid et al.* teaches, discloses or suggests a signal level detection circuit coupled to *the input terminals of the CPU or the Northbridge.* In this regard, in FIG. 1 of *Habid et al.*, the shutdown control circuit 124 is coupled to the power supply 122 only, not coupled to processors 110a and 110b and the Northbridge 140. For this reason as well, claims 11 and 20 are deemed clearly to be allowable over the cited references, so that the rejection of claims 11 and 20 should be withdrawn.

New Claims

New claims 21 and 22 recite, in part, "wherein the flip-flop comprises a terminal coupled to the Southbridge." Support for the newly added claims may be found in the specification at page 6, lines 13-15:

> The disconnection and reconnection of LDT bus 22 are performed according to the voltage level of the signal LDTSTOP# *output by the Southbridge 28,*

and at page 7, lines 7-16:

> the signal LDTSTOP_STATUS output by the terminal Q of the flip-flop 40 is reset to "0" when the voltage level of *the signal LDTSTOP# received by the terminal RST of the flip-flop 40* becomes a low voltage level. The level of the signal LDTSTOP# is high in its normal state. The logic level of the signal LDTSTOP_STATUS output by the terminal Q of the flip-flop 40 is low "0" after assertion and de-assertion of the signal LDTSTOP# in sequence. Thus, the asserted and de-asserted process of the signal LDTSTOP# is detected.

Applicants therefore believe that the limitation of "the flip-flop comprises a terminal coupled to the Southbridge" is supported in the specification.

This limitation in new claim 21-22 also further distinguishes the invention over the prior art. Neither *AAPA* nor *Habid et al.* teaches, discloses or suggests that a *flip-flop comprises a terminal coupled to the Southbridge.*

In *Habid et al.*, the Southbridge is coupled between the power supply and the power pushbutton, not coupled to the flip-flop. That is, the Southbridge 162 is coupled between the power supply 122 and the power pushbutton 224. In this regard, see line 65 of Column 3~ line 5 of Column 4, which states

> Generally, a power pushbutton **224** is coupled to an interface, e.g. south bridge **162**, and it is used to turn the power supply **122** on and off. For example, when the power pushbutton **224** is momentarily pushed, a signal is sent to the south bridge **162** which in turn supplies either a logic high or logic low signal to input **220** (PS_ON#), turning off or on the power supply **122.**

See also FIG. 2 of *Habid et al.* which clearly show that the Southbridge 162 is not coupled to the flip-flop 214. Thus, the Applicants believe it clear that this limitation is not taught by the cited references. For this reason alone, the Applicants believe that claims 21-22 clearly are allowable over the cited references.

Conclusion

For the reasons as described above, it is submitted that claim 1 is allowable over the *AAPA*. Insofar as claim 1 is allowable, claims 2-11 and 21, all depending from claim 1, also are allowable, and these dependent claims are further deemed to be allowable for the reasons of their further distinguishing recitations as discussed above. For the same reason, Applicants believe that claim 12 and depending claims 13-20 and 22, are also allowable.

Based on the above, it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 1-22, earnestly is solicited.

Should Examiner feel that discussion of the application and the Amendment would be conducive to the prosecution and allowance thereof, applications respectfully request that the Examiner kindly contact the undersigned at the telephone listed below to arrange for such a discussion.

Respectfully submitted,

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Date

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